

Loop Compensation Design Case Study: Buck DC-DC Switching Converter

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Abstract

This paper develops a buck converter design example using different compensation methods to ensure closed loop stability and to optimize system performance. Various compensators are designed using asymptotic Bode plots based primarily on loop bandwidth and stability margins. Computer simulation results are included to show time domain step response behavior and to verify performance improvements.

1 Introduction

The buck converter is a switch mode, DC-DC, power supply. It accepts a source voltage, V_g and produces a lower output voltage, V with high efficiency. An important component of a practical buck converter is control feedback which assures a constant output voltage and attenuates unwanted disturbances. The feedback loop of a buck converter presents several challenges which are explored in the compensation examples.

In this paper we present a series of example buck converter feedback compensation approaches. The design of the buck converter circuit is kept constant to allow comparison of the effects of different compensation schemes. The primary tool that will be applied to evaluate the different compensation approaches are asymptotic Bode plots which are drawn based on corner frequencies of each block in the regulator system. This methodology provides a quick and efficient assessment of circuit performance and an intuitive sense for the trade offs for each compensation approach. Bode plots also directly illuminate the two critical loop stability characteristics, gain and phase margin (GM and PM respectively).

Additional analysis of each compensation approach is undertaken through computer simulation. The PECS [1] circuit simulator is used to evaluate the

effects of V_g transients, a common problem in real power supply designs. A Matlab [2] simulation is also performed to validate the manual Bode analysis and to determine the exact gain and phase margin. Finally a closed loop Matlab simulation is used to show the ability of the feedback system to attenuate undesired effects as a function of frequency.

We explore the following topics in the remainder of the paper:

Section 2 Buck converter system model

Section 3 Behavior of an uncompensated buck converter

Section 4 Dominant pole compensation

Section 5 Dominant pole compensation with zero

Section 6 Lead compensation

Section 7 Dominant pole with lead compensation

Section 8 Extended bandwidth design

Section 9 Conclusion and summary

Appendix Additional supporting materials

2 Buck Converter System Models

2.1 General Model [3]

Figure 1 is a block diagram of the system components of a buck converter with feedback. The converter power stage accepts V_g as its power source and the control input $d(s)$ to produce the output voltage V . The feedback sensor $H(s)$, monitors the converter output voltage which is then compared with a reference voltage V_{ref} . The difference output of these two voltages is provided to the feedback compensation circuit $G_c(s)$ and then to the pulse width modulator (PWM) which produces the control waveform for the switching converter $d(s)$. The resulting loop gain is thus given by

$$T(s) = G_c(s) \left(\frac{1}{V_M} \right) G_{vd}(s) H(s) \quad (1)$$

2.2 Simplified System Model

The general buck converter block diagram provides a complete model for analysis of converter. However, for our analysis we will use a simplified model show in Fig. 2 which includes only the elements required for the analysis we will provide. We do not evaluate any source of disturbance except V_g transients.

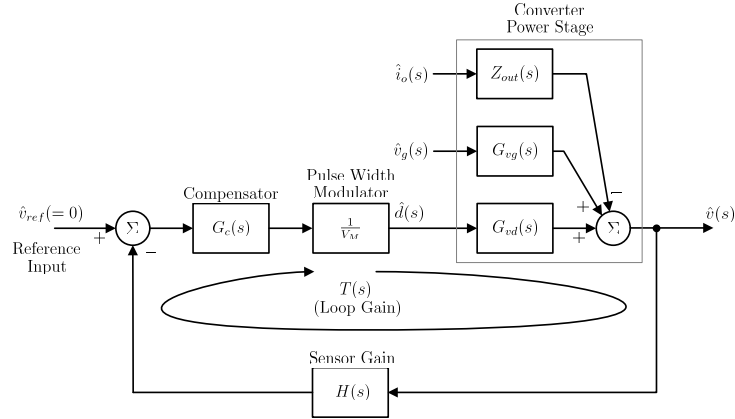


Figure 1: Generalized Power System Model

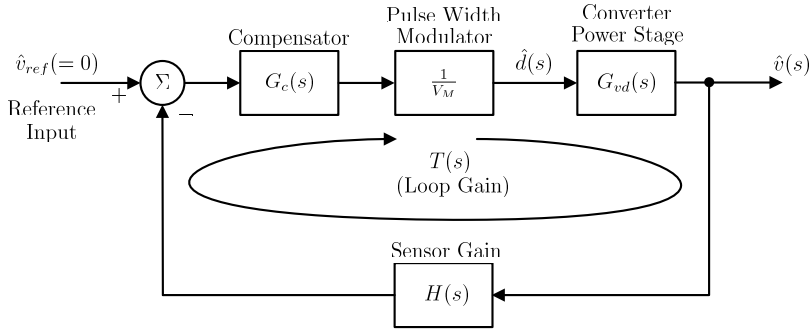


Figure 2: Simplified System Diagram

2.3 Design Targets

To facilitate easy comparison between the selected compensation schemes, the design of the buck converter is fixed with specified values. These values are specified in Table 1.

2.4 Buck Converter Model Analysis

Figure 3 shows a schematic model for the power converter block. The LCR is a second order circuit with a transfer function described by equation (2). It has a resonant frequency value, $\omega_o = 6.28Krad/s$ or $f_o(= \frac{\omega_o}{2\pi}) = 1.0$ kHz from (3) and a Q of 9.5 from (4). The low frequency gain of the converter is equal to V_g which is specified to be 28V.

Table 1: Specified values

Name	Value	Description
V_g	28V	Input Voltage
V	15V	Output Voltage
I_{load}	5A	Load current
L	50uH	Buck inductor value
C	500uF	Buck capacitor value
V_m	4V	PWM ramp amplitude
$H(s)$	1/3	Sensor gain
f_s	100kHz	PWM frequency

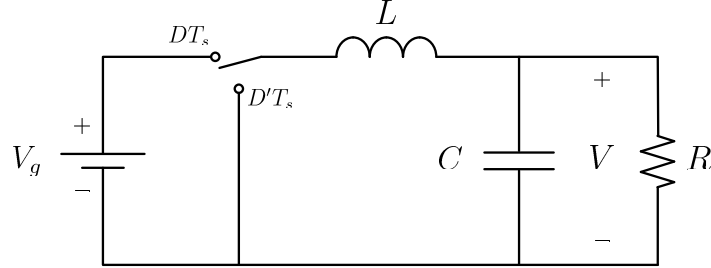


Figure 3: Converter Power Stage

$$G_{vd}(s) = V_g \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (2)$$

$$\omega_o = \frac{1}{\sqrt{LC}} \quad (3)$$

$$Q = R\sqrt{\frac{C}{L}} \quad (4)$$

Consider the transfer function $v(s)/v_d(s)$ of the low pass filter formed by the LCR network. The switching frequency $f_s = 100\text{kHz}$ is much higher than the resonant frequency $f_0 = 1\text{kHz}$ of the LCR network. During circuit operation, the switch toggles the LCR input between V_g and ground with a duty cycle D determined by the feedback loop. A Fourier analysis of the LCR input waveform includes an average DC component $V = DV_g$ and an f_s fundamental component and its harmonics as typified by a rectangular waveform. The LCR acts as a low pass filter with a cut off frequency equal to f_o . It passes the DC component to the output but attenuates f_s and its harmonics.

3 Uncompensated System

It is instructive to start our evaluation with an uncompensated open loop converter, one with a $G_c(s) = 1$. The loop gain is then given from (1) as

$$T(s) = \frac{T_o}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_o}\right)^2} \quad (5)$$

where

$$T_o = \frac{V_g H(0)}{V_m} \quad (6)$$

To construct a Bode plot we use the values from equations (2)-(4) to establish the shape of the Bode magnitude plot. The low frequency gain given by (6) has a value of 2.33. The magnitude around f_o peaks due to the resonant Q of 9.5. At frequencies above f_o the gain declines at -40dB/decade.

The Bode phase plot is determined only by $G_{vd}(s)$. It has a low frequency phase shift of 0° . At $f_o 10^{-\frac{1}{2Q}}$ or 886Hz (≈ 900 Hz), the phase turns negative and at f_o the phase has reached -90° . The phase continues to become more negative until it reaches -180° at $10^{\frac{1}{2Q}}$ or 1129Hz (≈ 1.1 kHz). At frequencies higher than 1.1kHz the phase remains at -180° .

From the Bode plot it can be determined that unity gain occurs at a frequency, $f = f_c$ such that

$$T_o \left(\frac{f_o}{f_c}\right)^2 = 1 \quad (7)$$

which with $T_o=2.33$ and $f_o=1$ kHz, results in $f_c=1.5$ kHz. At this frequency the phase is -180° providing zero phase margin. The phase asymptotes show that phase does not cross the -180° phase level (but is asymptotic to it) which implies that the gain margin is infinite. Figure 5 is a Matlab margin plot indicating the actual unity gain frequency to be 1.8 kHz with a phase margin of 4.7° . Also, the Matlab analysis indicates an infinite gain margin.

Figure 6 shows a PECS implementation of the open loop buck converter system. The input to the modulator is set to 2.1V which results in the target steady state duty ratio of $D = V_g = \frac{15}{28} = 0.54$ required to set the output voltage at $V = 15$ V for a nominal input voltage of $V_g = 28$ V.

Figure 7 shows the output voltage response of the open loop system shown in Figure 6 for voltage steps in V_g of 28V \rightarrow 30V \rightarrow 28V. The response is indicative of the high resonance Q of 9.5 at the resonant frequency $f_o=1$ kHz. Note also that at an input voltage of $V_g=30$ V the output voltage settles at $V = DV_g = 0.54 \times 30 = 16.2$ V, as shown in Fig. 7.

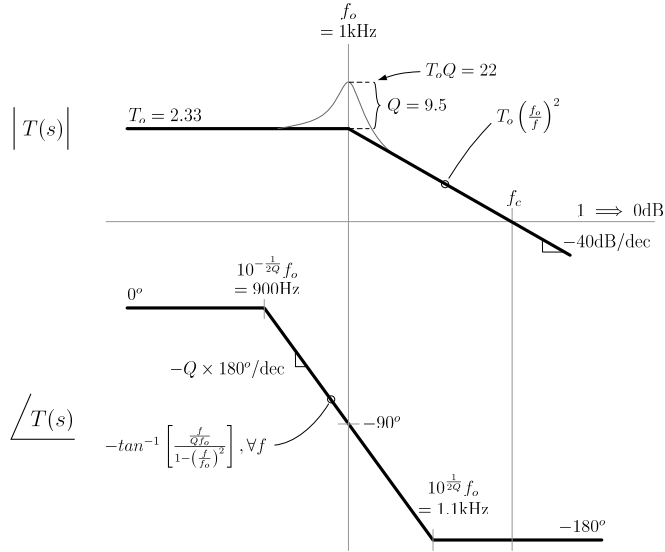


Figure 4: Uncompensated Gain and Phase Plot

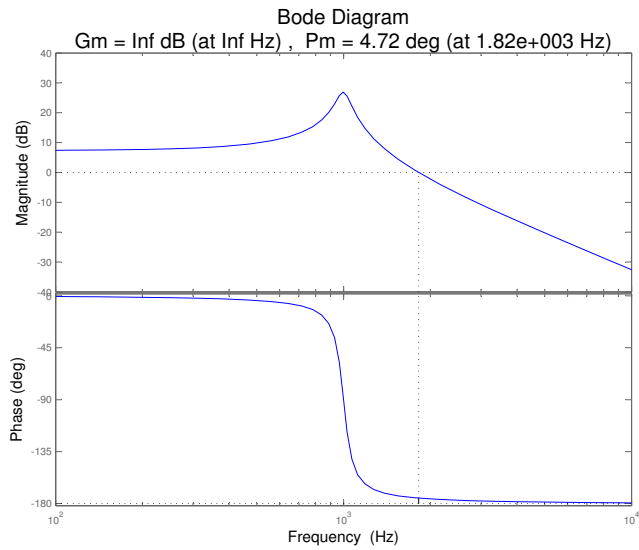


Figure 5: Matlab Uncompensated Bode plot

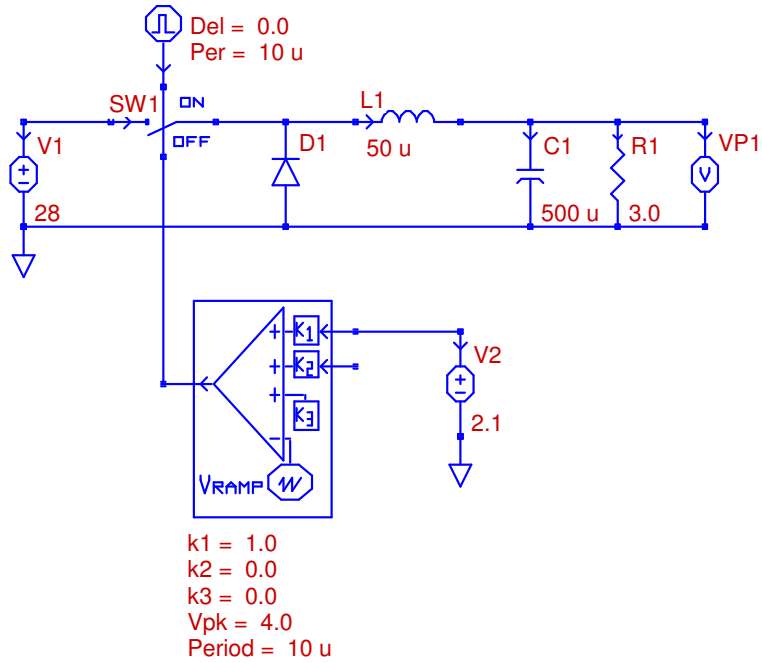


Figure 6: PECS Schematic of Open Loop System

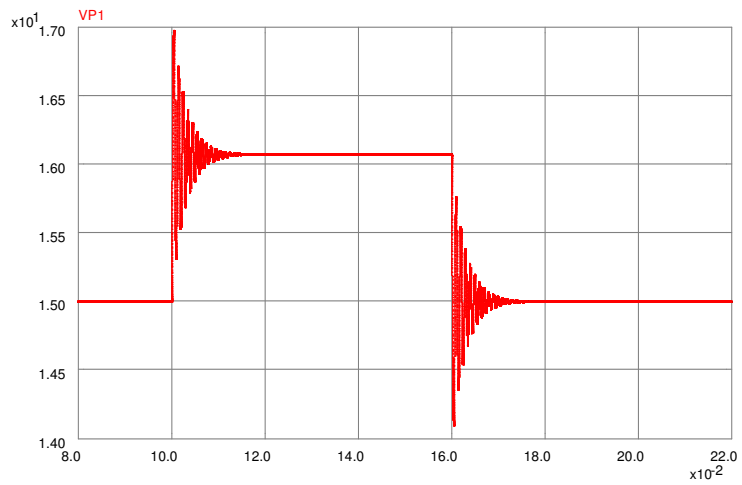


Figure 7: PECS Simulation of Open Loop System

4 Dominant Pole Compensation

Dominant pole compensation is one of the simplest and most common forms of feedback compensation. The motivating idea behind this type of feedback control is to shape the open loop gain of the system such that two objectives are achieved:

1. High gain is achieved at DC and low frequencies. This condition ensures low steady state error.
2. The gain at the plant's lowest frequency pole is less than or equal to 0dB. This condition ensures a positive phase margin and, consequently, stability.

In the case of dominant pole compensation, these objectives are achieved using a compensator consisting of a single pole at a frequency well below those of the plant's poles. For the purposes of this example, an integrator, which is just a pole at DC, is employed

$$G_c(s) = \frac{\omega_I}{s} \quad (8)$$

where $\omega_I (= 2\pi f_i)$ is an appropriately chosen design constant. Figure 8 shows the Bode plot asymptotes for the magnitude and phase of this compensator.

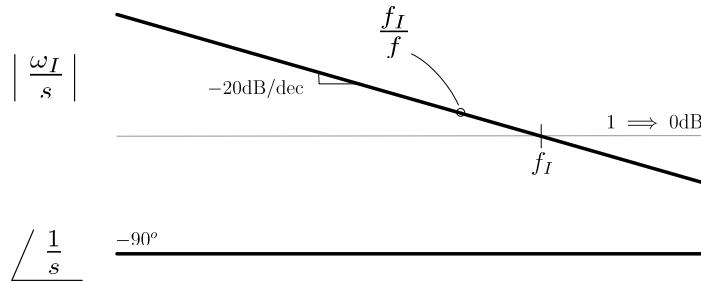


Figure 8: Bode Plot of Dominant Pole Compensator

Design of the compensator now consists of selecting an appropriate compensator parameter, f_I . Following the previously stated criteria, this is a matter of choosing the largest compensator gain such that the total gain at the lowest frequency plant pole(s) is less than 0dB. The loop gain of the system with this compensator is given by

$$T(s) = \frac{\omega_I T_o}{s \left[1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0} \right)^2 \right]} \quad (9)$$

Figure 9 shows the graphical construction of the phase asymptotes for the loop gain with the compensator. Note that because the plant's dominant pole is second order, it contributes a phase shift of -180° at high frequencies and a shift of exactly -90° at f_o . Furthermore, the compensator contributes its own -90° phase shift and does so for all frequencies. Consequently, the total phase shift of the compensated open loop transfer function is -180° at the dominant pole frequency, f_o . For this reason it is prudent to design in some additional gain margin. A value of 3dB is initially chosen for this analysis.

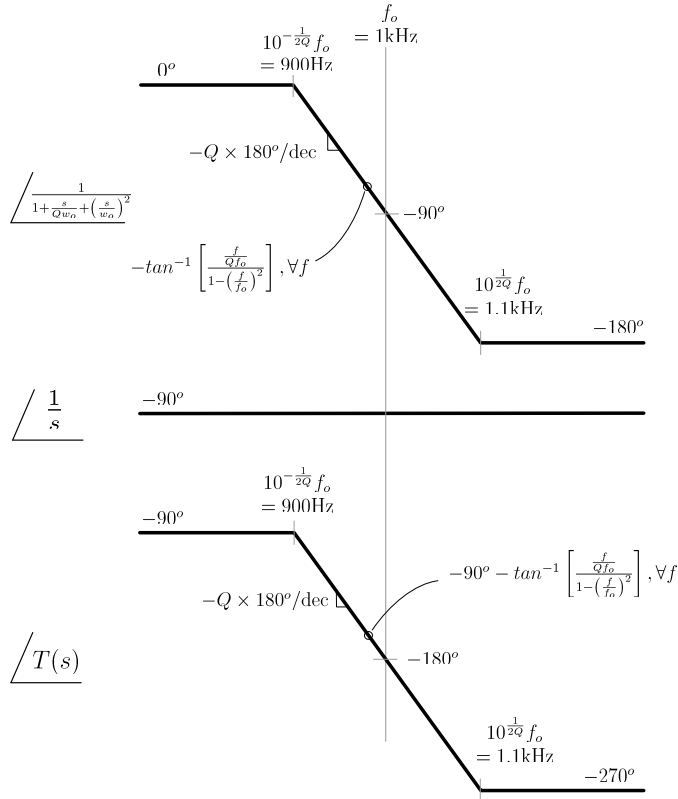


Figure 9: Graphical Construction of Phase Asymptotes for Dominant Pole Compensated Open Loop

Figure 10 shows how the plant and compensator transfer functions combine to produce the gain of the compensated open loop. To achieve a loop gain that is -3dB at f_o , we require the magnitude at f_o to equal 0.7

$$\frac{f_I T_o Q}{f_o} = 0.7 \quad (10)$$

For $T_o = 2.33$ and $f_o = 1.0\text{kHz}$, we find $f_I = 32$.

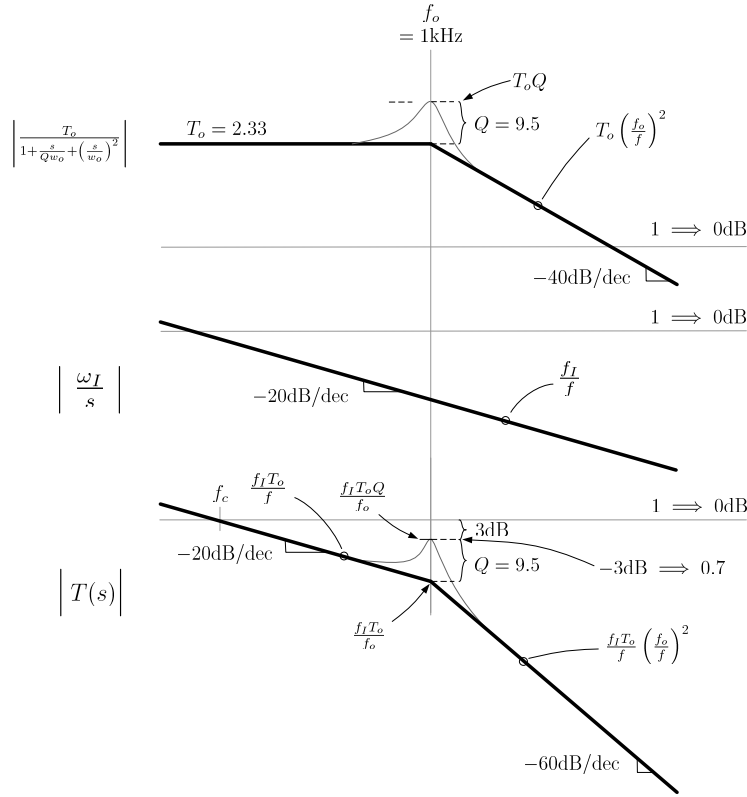


Figure 10: Graphical Construction of Gain Asymptotes for Dominant Pole Compensated Open Loop

Figure 11 shows the Bode plot of the resulting gain and phase asymptotes and Figure 12 shows a Matlab margin analysis which confirms the design.

With a compensator designed and verified via Matlab, the next stage is to design a circuit that implements the compensator. Figure 13 shows the general

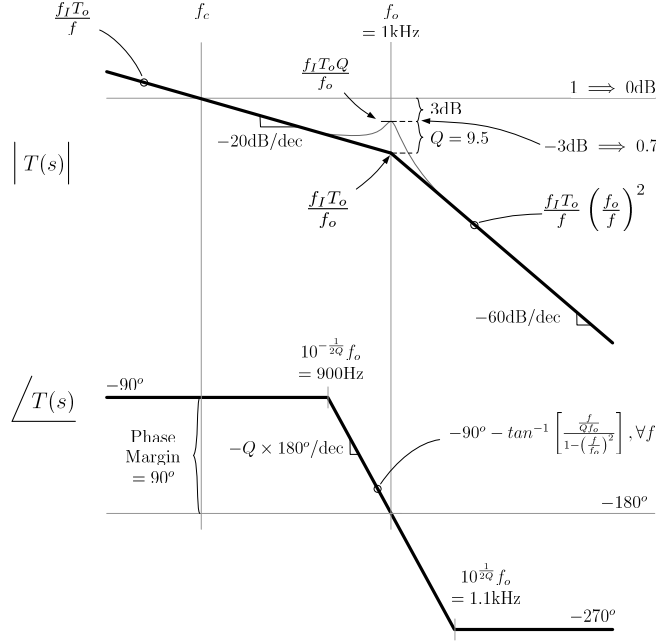


Figure 11: Open Loop System Gain and Phase with Dominant Pole Compensation

form of an operational amplifier in a integrator configuration. The transfer function for this circuit is given by:

$$G(s) = \frac{-1}{(s/\omega_o)} \quad (11)$$

where

$$\omega_o = \frac{1}{RC} \quad (12)$$

where ω_o is the frequency at which the integrator gain is unity.

A capacitor value of 50nF is chosen for C . This value is within the range of low-cost, commercially available ceramic capacitors and is small enough to avoid any op-amp slew rate issues. Equating ω_o with the compensator parameter, ω_I ($= 2\pi f_I$) and solving for R gives

$$R = \frac{1}{\omega_I C} = \frac{1}{2\pi(32)(50\text{nF})} \approx 100\text{k}\Omega \quad (13)$$

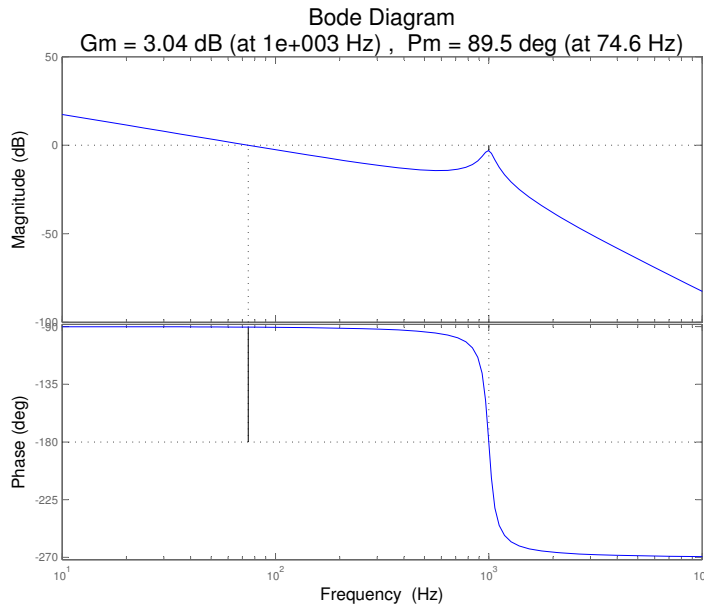


Figure 12: Matlab Analysis of Dominant Pole Compensator

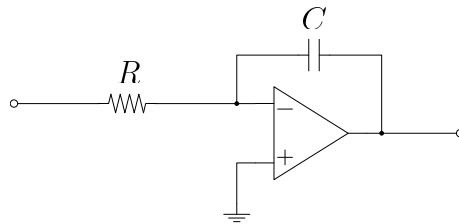


Figure 13: Op-Amp Integrator Circuit

A PECS simulation is created to verify the time domain performance of the implementation. Figure 14 shows the complete PECS circuit model for the design.

Figure 15 shows the results of the PECS simulation for a 2V disturbance on the supply voltage, V_g . The input voltage steps are $28V \rightarrow 30V \rightarrow 28V$. The simulation exhibits several undesirable characteristics:

1. The regulator does a poor job of rejecting the input voltage disturbance. Nearly all of the input voltage excursion shows up as a transient on the output.
2. The regulator exhibits a substantial amount of ringing in response to the

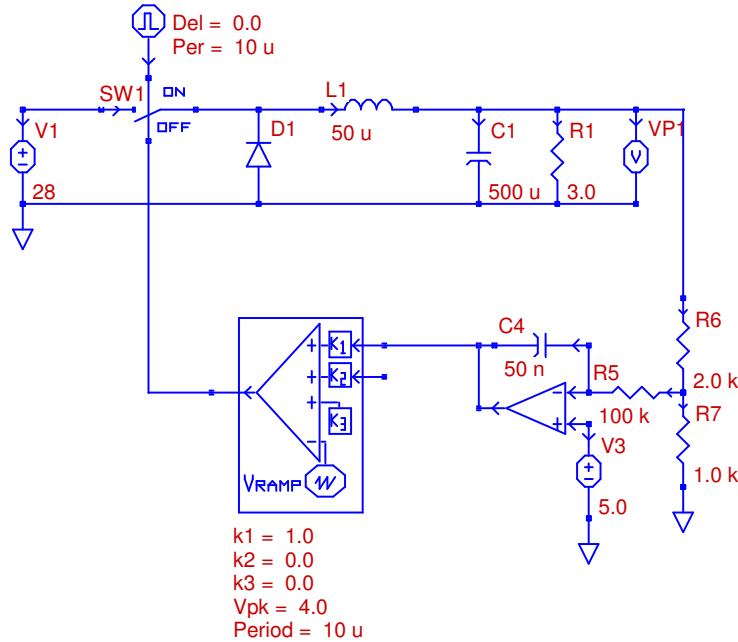


Figure 14: PECS Schematic of Dominant Pole Compensated System

input disturbance. Closer examination of the ringing, as shown in Figure 16, reveals that the frequency of the oscillations is the same as the resonant frequency of the plant, f_o , and is not the result of defective control loop design.

It is clear from the simulation results that, although the design is stable and exhibits zero steady-state error, there is much room for improvement, particularly with respect to its transient response.

One additional experiment is performed using the dominant pole compensation scheme. The Q of the plant's dominant pole is reduced by placing a large capacitor in series with a small damping resistance. Figures 17 and 18 show the PECS circuit schematic and simulation results, respectively.

One can see clearly that the ringing of the previous design has been eliminated. Unfortunately, the poor rejection of input voltage transients remains.

Furthermore, this is probably not an ideal solution from a practical standpoint. The large value capacitor will be relatively expensive in terms of com-

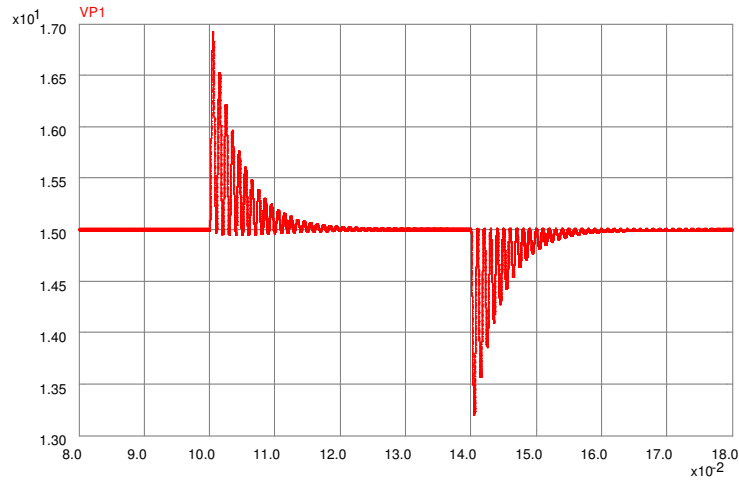


Figure 15: PECS Simulation of Dominant Pole

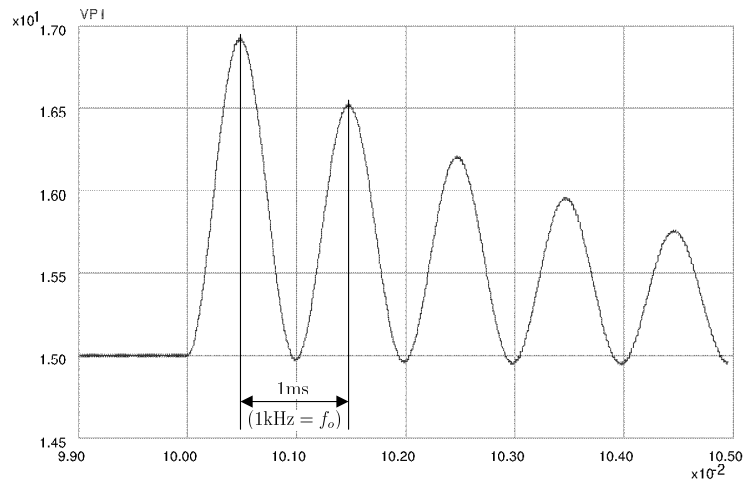


Figure 16: Pole of Dominant Pole Simulation Showing Oscillation at Resonant Frequency

ponent price and physical space. Alternate compensation schemes still offer the potential for better performance at lower cost.

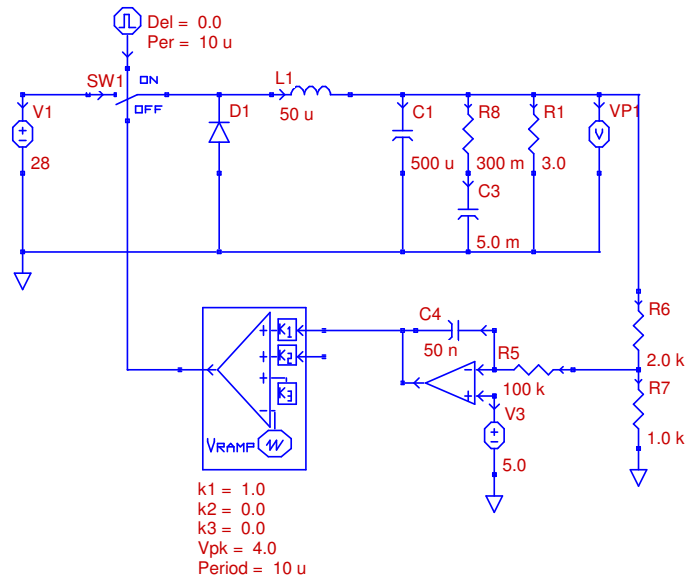


Figure 17: PECS Schematic of Dominant Pole with Damping

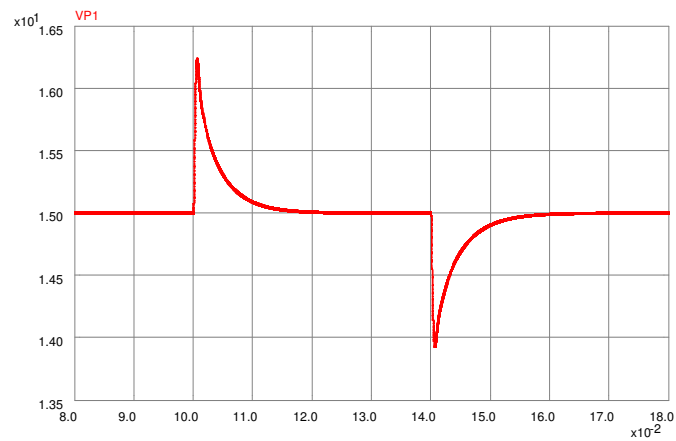


Figure 18: PECS Simulation of Dominant Pole with Zero Compensation and Damping

5 Dominant Pole Compensation with Zero

The dominant pole compensator of the previous section, while stable and having zero steady state error, exhibits several undesirable characteristics including poor rejection of input supply voltage excursions and pronounced ringing in response to transients. One might assume that these issues are related to the minimal, 3dB, gain margin for which the compensator was designed. This section explores that line of reasoning by modifying the compensator of the previous section in order to substantially increase the gain margin.

The dominant pole compensator is modified by adding a zero at the resonant frequency of the plant and by reducing the gain to -10dB. Overall gain margin is improved in two ways:

1. by directly increasing the gain margin at the resonant frequency, f_o , from 3dB to 10dB.
2. by shifting the frequency at which the phase reaches -180° beyond the resonant frequency and the gain peak due to the plant's Q.

The form of the modified compensator transfer function is:

$$G_c(s) = \omega_I \frac{1 + s/\omega_z}{s} \quad (14)$$

We will use $\omega_z = \omega_o$ or $f_z (= \frac{\omega_z}{2\pi}) = f_o$. Which results in a loop gain of

$$T(s) = \omega_I \frac{1 + s/\omega_o}{s} \frac{T_o}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2} \quad (15)$$

Figure 19 shows the resulting Bode plot asymptotes. We would like to set the gain at f_o to $1/\sqrt{10}$ (which corresponds to -10dB). From the magnitude plot we see that we want

$$\frac{f_I T_o Q}{f_o} = \frac{1}{\sqrt{10}} \quad (16)$$

which given $T_o = 2.33$, $Q = 9.5$, $f_o = 1kHz$, results in $f_I = 14.3$. Figure 20 shows a Matlab confirmation of the Bode plot. Note that a gain margin of 11dB is predicted at a phase cross-over frequency of 1.06kHz, slightly higher than the plant's resonant frequency.

Figure 21 shows a standard op-amp implementation with the desired transfer function. The transfer characteristics of the circuit are given by:

$$G(s) = -A \frac{1 + s/\omega_1}{\frac{s}{\omega_1}} \quad (17)$$

where:

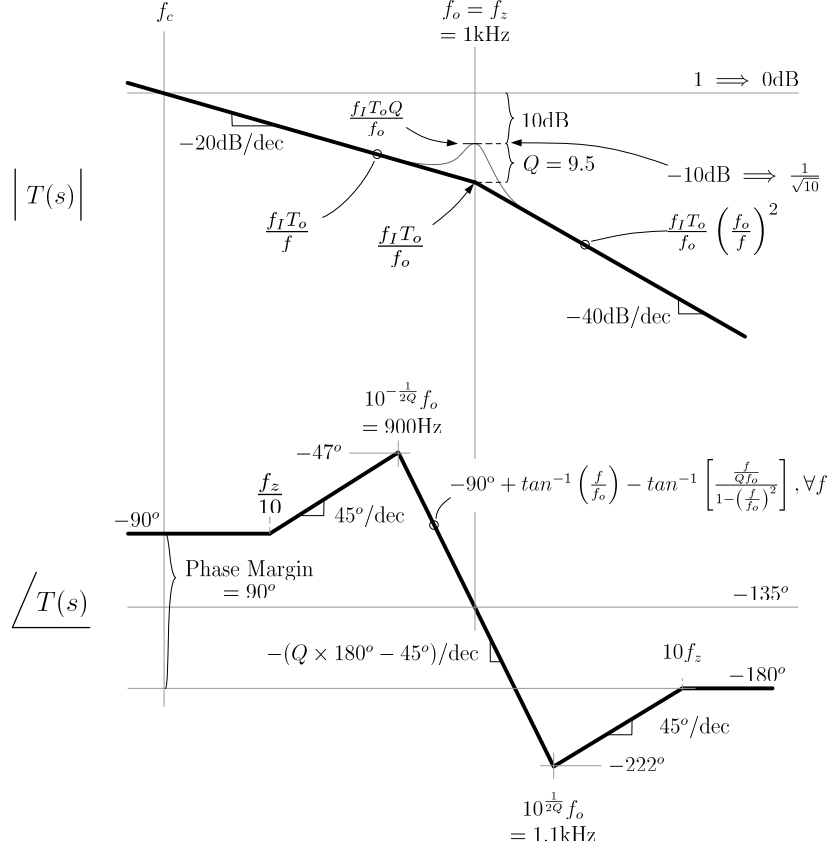


Figure 19: Open Loop System Gain and Phase with pole-zero Compensation (10dB GM)

$$A = \frac{R_2}{R_1} \quad \text{and} \quad \omega_1 = \frac{1}{R_2 C_1} \quad (18)$$

Equating $f_1 (= \frac{\omega_1}{2\pi})$ to the plant resonant frequency, f_o and ω_I to $A\omega_1$ provides two equations with three unknowns. Choosing, somewhat arbitrarily, a value of 100k for R_1 , leads to the following values.

$$R_2 = \frac{f_I R_1}{f_1} = \frac{(14.3)(100\text{k}\Omega)}{(1\text{k}\Omega)} = 1.4\text{k}\Omega \quad (19)$$

$$C_1 = \frac{1}{\omega_1 R_2} = \frac{1}{2\pi(1\text{kHz})(1.4\text{k}\Omega)} = 110\text{nF} \quad (20)$$

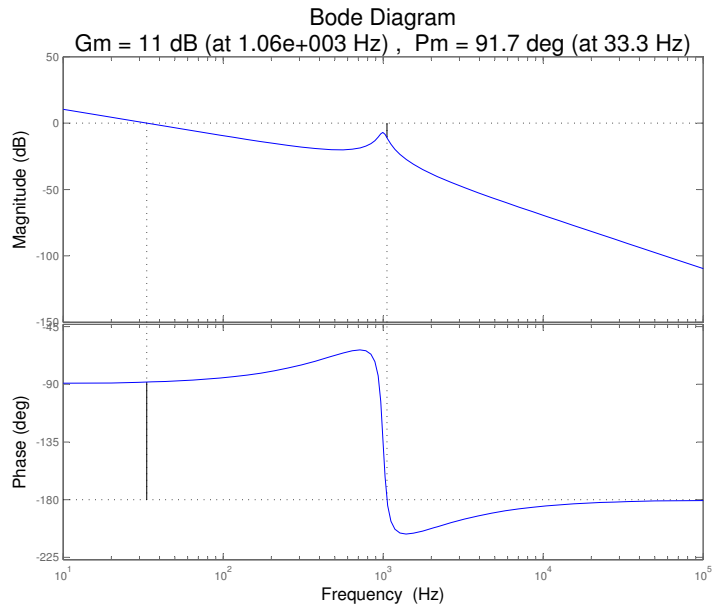


Figure 20: Matlab Analysis of Dominant Pole Compensator with Zero

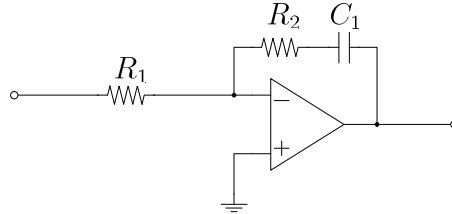


Figure 21: op-amp Integrator with Zero

Figure 22 shows a PECS circuit implementation of the system with the new compensator. Figure 23 shows the response of the system to a transient on the input voltage.

The modified compensator shows little improvement over the original circuit. It still fails to provide good rejection of input voltage transients and the previously observed ringing is still present.

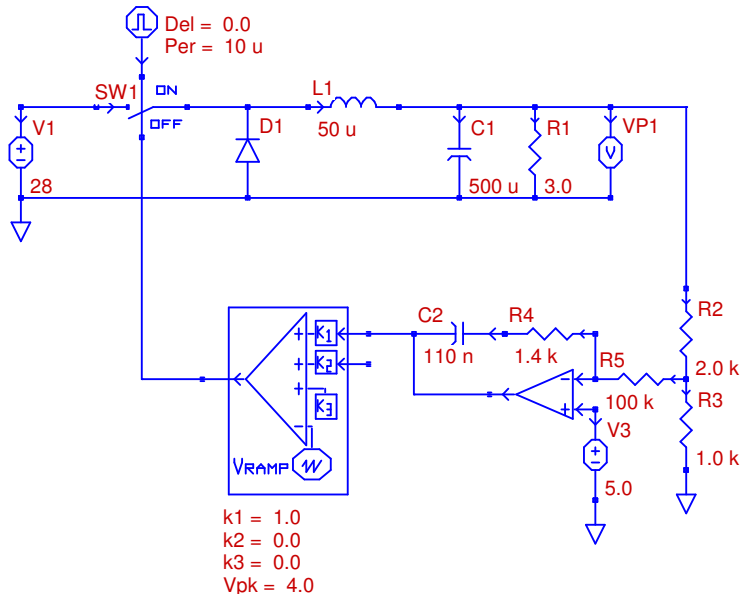


Figure 22: PECS Schematic of Dominant Pole with Zero Compensation (10 dB GM)

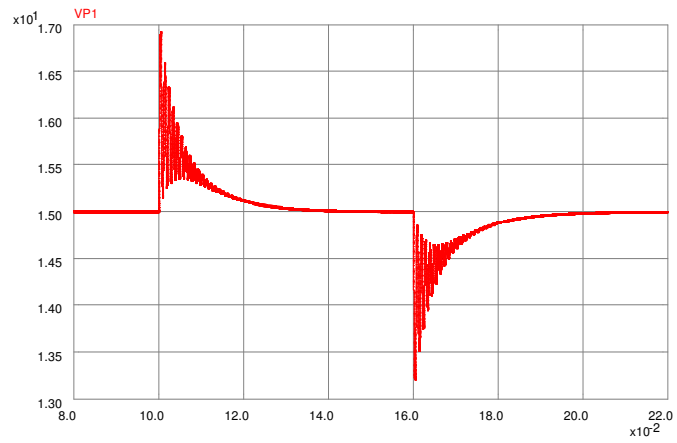


Figure 23: PECS Simulation of Dominant Pole with Zero Compensation (10 dB GM)

6 Lead Compensation

A more sophisticated way to improve the performance of the buck converter is with a lead compensator. The transfer function of this compensator is

$$G_c(s) = G_{c_o} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)}, \quad (21)$$

where $\omega_z < \omega_p$. As can be seen from the plot of the transfer function shown in Figure 24, the lead compensator provides both a phase boost that is adjustable based on the pole and zero frequencies, and a gain boost at higher frequencies that can result in a higher crossover frequency for a lead-compensated buck converter. Generally, a lead compensator is used to provide a phase boost, the level of which is chosen to improve the phase margin to a desired value. The new crossover frequency can be chosen arbitrarily. The design shown here will be to obtain a 45° phase margin and a crossover frequency of 5 kHz for the loop gain with a lead compensator.

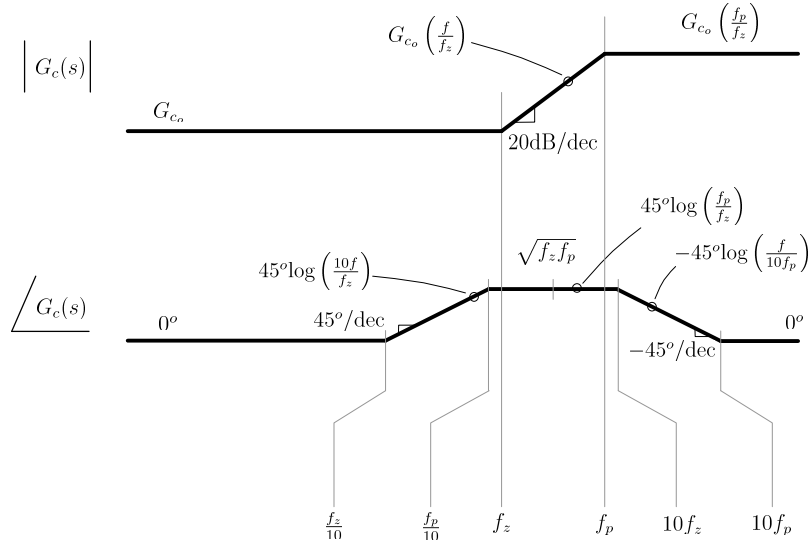


Figure 24: Bode Plot of Lead Compensator

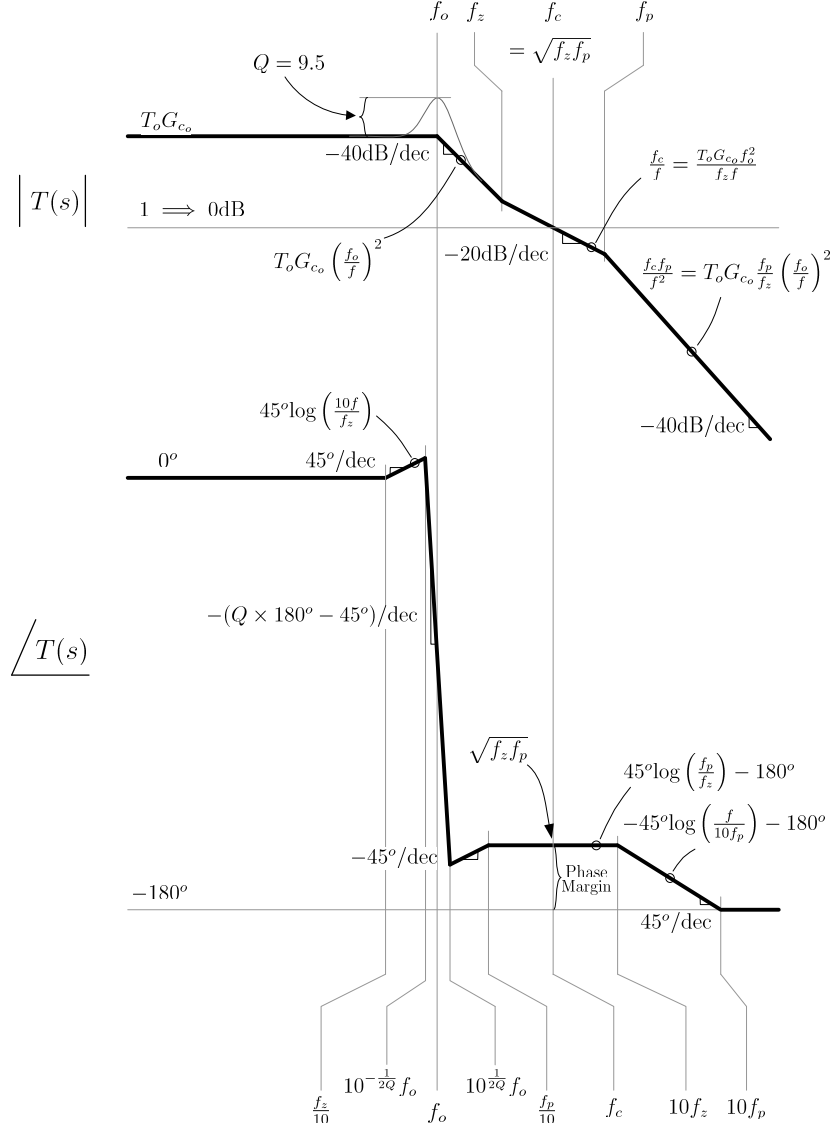


Figure 25: Bode Plot of Lead Compensated System

When the compensator is placed in the loop, the loop gain of the buck converter system becomes

$$T(s) = T_0 G_{c_0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right) \left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)} \quad (22)$$

The asymptotic Bode plot of this loop gain is shown in Fig. 25. The expressions shown can be used to place the pole and zero frequencies of the compensator to obtain the desired phase margin and unity-gain crossover frequency. As can be seen, the phase margin of the lead compensated system is given by

$$\phi_M = 45^\circ \log \left(\frac{f_p}{f_z} \right)$$

For a desired phase margin of 45° we have

$$45^\circ = 45^\circ \log \left(\frac{f_p}{f_z} \right)$$

or

$$f_p = 10f_z$$

Also, the crossover frequency, f_c will necessarily be the geometric mean of the pole and the zero frequency. Since the phase margin condition gives a relationship between the pole and zero frequencies, this can be used to solve for both.

$$f_c = \sqrt{f_z f_p}$$

$$5 \text{ kHz} = \sqrt{10f_z^2}$$

$$f_z = \frac{5 \text{ kHz}}{\sqrt{10}}$$

$$f_z = 1.58 \text{ kHz and } f_p = 15.8 \text{ kHz}$$

These relationships result in the pole and zero frequencies for the lead compensator. To complete the design, the required low-frequency gain G_{c_o} of the compensator to place the unity-gain point at the appropriate frequency must be determined. This can be found by equating the values of the gain asymptotes at f_z .

$$T_0 G_{c0} \left(\frac{f_0}{f_z} \right)^2 = \frac{f_c}{f_z}$$

Substituting the values of f_o and T_o for the example converter, and the values of f_z and f_c as previously calculated, the gain G_{c_o} of the compensator is

$$G_{c_o} = \frac{1}{T_0} \left(\frac{f_z}{f_0} \right)^2 \frac{f_c}{f_z}$$

$$G_{c_o} = \frac{1}{2.33} \left(\frac{1.58 \text{ kHz}}{1 \text{ kHz}} \right)^2 \frac{5 \text{ kHz}}{1.58 \text{ kHz}}$$

$$G_{c_o} = 3.4$$

As seen in previous designs and now in the phase plot of Fig. 25, the phase response is asymptotic to -180° at high frequencies and so does not cross through this level which implies an infinite gain margin.

In summary, we have designed a lead compensator which, using asymptotic Bode plot approximations, result in a 45° phase margin with a unity gain frequency of 5kHz and an infinite gain margin. The Matlab simulation in Figure 26 verifies the results, above.

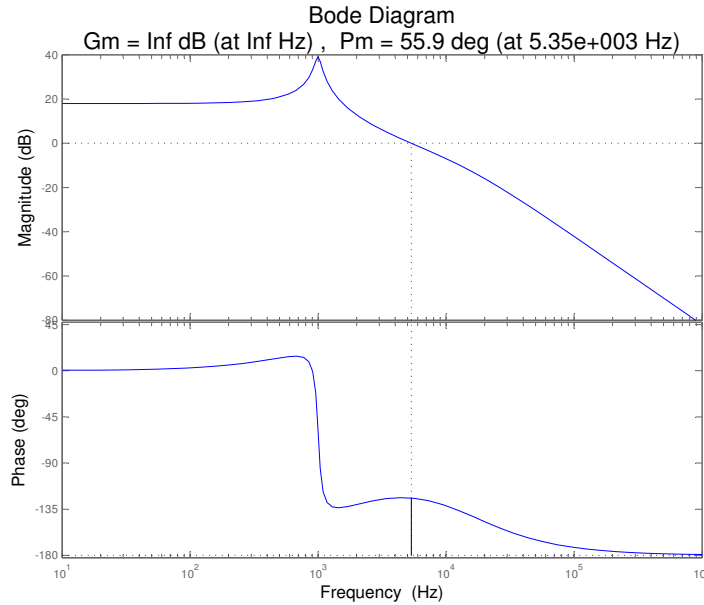


Figure 26: Matlab Lead Compensator

With all of the parameters of the lead compensator determined, what remains is to implement the compensator using an op-amp circuit and simulate the closed-loop converter to evaluate its performance. A general circuit that can be used to implement any lead or lag compensator is shown in Fig. 27. The transfer function of this circuit is

$$G_c(s) = G_{c_o} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \quad (23)$$

where

$$G_{c_o} = -\frac{R_2}{R_1} \quad (24)$$

$$f_z = \frac{\omega_z}{2\pi} = \frac{1}{2\pi R_1 C_1} \quad (25)$$

$$f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi R_2 C_2} \quad (26)$$

The resistor ratio sets the low frequency gain, and the two resistor-capacitor pairs set the pole and zero frequencies. Using standard resistor values of $R_1 = 100 \text{ k}\Omega$ and $R_2 = 330 \text{ k}\Omega$ results in the required low frequency gain of close to $G_{c_o} = 3.4$. Using (23) we find

$$C_1 = \frac{1}{2\pi (1.58 \text{ kHz}) (100 \text{ k}\Omega)} \Rightarrow C_1 = 1.0 \text{ nF}$$

$$C_2 = \frac{1}{2\pi (15.8 \text{ kHz}) (330 \text{ k}\Omega)} \Rightarrow C_2 = 33 \text{ pF}$$

It is also necessary to derive a value for the reference voltage on the non-inverting input of the op-amp. The sensed voltage from the output will be 5 V in steady-state as before, and the control voltage should be 2.14 V. Using these in combination with the resistor values for the lead compensator, the reference voltage can be found.

$$V_{ref} = \frac{R_2}{R_1 + R_2} V_{sense} + \frac{R_1}{R_1 + R_2} V_{control}$$

$$V_{ref} = \frac{330 \text{ k}\Omega}{100 \text{ k}\Omega + 330 \text{ k}\Omega} (5 \text{ V}) + \frac{100 \text{ k}\Omega}{100 \text{ k}\Omega + 330 \text{ k}\Omega} (2.14 \text{ V}) = 4.33 \text{ V}$$

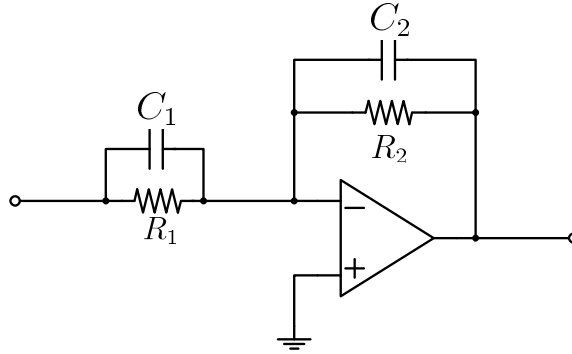


Figure 27: op-amp circuit implementation of lead compensator

Using these values in the PECS simulator (see Figure 28 for PECS schematic), the response of the lead-compensated buck converter to a step in the input voltage was simulated as before. The results of the simulation are shown in Figure 29. The lead compensator is quite effective in increasing the phase margin of the system. The oscillatory behavior evident in the output voltage of the uncompensated converter is not present, and the magnitude of the steady-state error due to the step is reduced, though not eliminated. Thus, the system with the lead compensator is very stable, but will still exhibit steady-state errors to a step disturbance. To fix this problem, the system type number must be

increased by adding a pole at $s = 0$, as was seen previously. This is the approach taken in the design of the subsequent compensators.

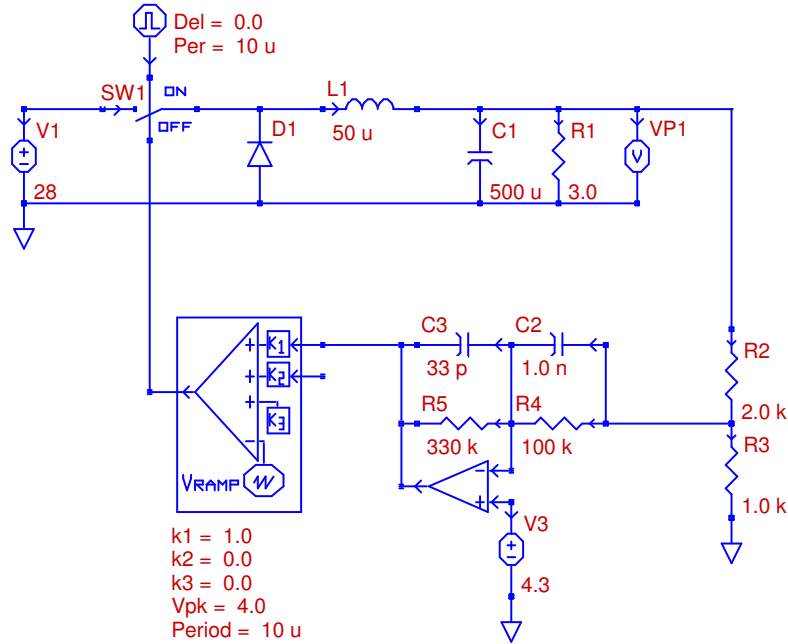


Figure 28: PECS Schematic of Lead System

7 Dominant Pole with Lead Compensation

So far we have seen that with a dominant pole integral compensation a zero steady state error can be achieved at the expense of limited bandwidth with resulting large overshoot in the step response. In contrast lead compensation is able to extend bandwidth thus reducing step response overshoot. However, due to severely curtailed low frequency loop gain, a non-zero steady state error is seen.

In this section a compensator which is a composite of the two previous compensators is examined. The exact form of the compensator is:

$$G_c(s) = \frac{\omega_I \left(1 + \frac{s}{\omega_1}\right) \left(1 + \frac{s}{\omega_z}\right)}{s \left(1 + \frac{s}{\omega_p}\right)} \quad (27)$$

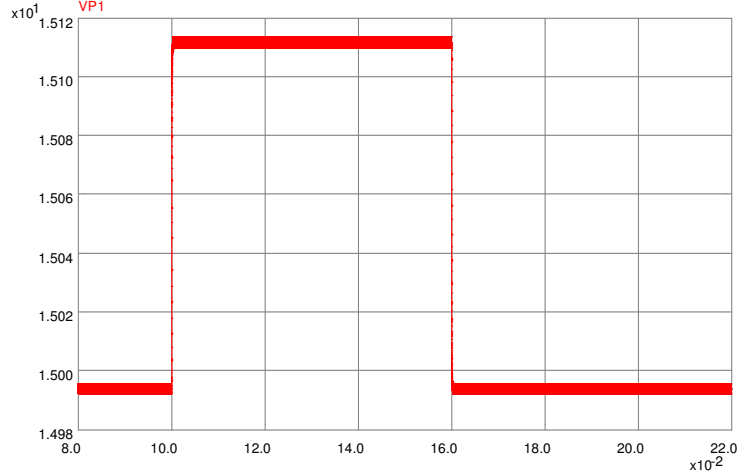


Figure 29: PECS Simulation of Lead System

Effectively, to the lead compensator design of the previous section we are adding an integrator pole, i.e. a pole at zero frequency, and a zero at $f_1 (= \frac{\omega_1}{2\pi})$. In the following we will consider two different values for the zero frequency f_1 .

In the first case f_1 will be chosen to be the largest frequency which, based on the phase asymptote, contributes $+90^\circ$ to the crossover frequency f_c , thus fully cancelling the -90° contribution from the integrator pole. This effectively leaves the phase margin unchanged from the lead compensator design of the previous section. From the phase asymptotes plots of a zero, we see that the zero frequency f_1 should be at $\frac{f_c}{10}$ which is 500Hz.

In the second design considered here we will lower the zero frequency to $f_1 = 150\text{Hz}$ and examine the effect on the closed loop performance.

In either case the expression for the loop gain is

$$T(s) = T_o \frac{\omega_I \left(1 + \frac{s}{\omega_1}\right) \left(1 + \frac{s}{\omega_z}\right)}{s \left(1 + \frac{s}{\omega_p}\right) \left[1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2\right]} \quad (28)$$

where f_1 is either 500Hz or 150Hz, as discussed above and $f_I (= \frac{\omega_I}{2\pi})$ is the only design variable to be determined.

7.1 Design 1: Zero $f_1 = 500\text{Hz}$

As before, asymptotic plots for the loop gain are drawn. As the construction of the phase plot is more involved than that of the magnitude plot, its construction is shown separately in Fig. 30. In Fig. 30, the top plot is that of the previous lead compensation design, as seen in Fig. 25. The plot of the phase of the component $\frac{1}{s} \left(1 + \frac{s}{\omega_1}\right)$ is shown in the center plot where $f_1 = 500\text{Hz}$. The final phase plot for the new loop gain is shown in the bottom plot. Both magnitude and phase plots for the new loop gain are shown together in Fig. 31.

To determine, f_I , the one unknown variable in the loop gain, we note that at the frequency f_1 the magnitude is set equal to the low frequency loop gain of the lead compensation design of the last section.

$$T_0 \frac{f_I}{f_1} = T_0 G_{c_o}|_{lead} \quad (29)$$

For $f_1 = 500$ we find $f_I = 1770$. Thus the expression for the compensator is as given in (27) with the following values

$$\begin{aligned} \omega_I &= 2\pi(1770) \\ \omega_1 &= 2\pi(800) \\ \omega_z &= 2\pi(1580) \\ \omega_p &= 2\pi(15800) \end{aligned} \quad (30)$$

To confirm the accuracy of the design, the Bode plot of the exact loop gain was evaluated using Matlab. This is shown in Fig. 32. Our asymptotic design values of crossover frequency f_c and phase margin of 5kHz and 45° , respectively were determined by Matlab as given by the Matlab "margin" command to be more precisely $5,370\text{Hz}$ and 50.5° , respectively, thus confirming the design procedure.

A compensator which realizes the transfer function is shown in Fig. 33 where we find

$$\begin{aligned} \omega_I &= \frac{1}{R_1(C_2 + C_3)} \\ \omega_1 &= \frac{1}{R_2 C_2} \\ \omega_z &= \frac{1}{R_1 C_1} \\ \omega_p &= \frac{1}{R_2 \frac{C_2 C_3}{C_2 + C_3}} \end{aligned} \quad (31)$$

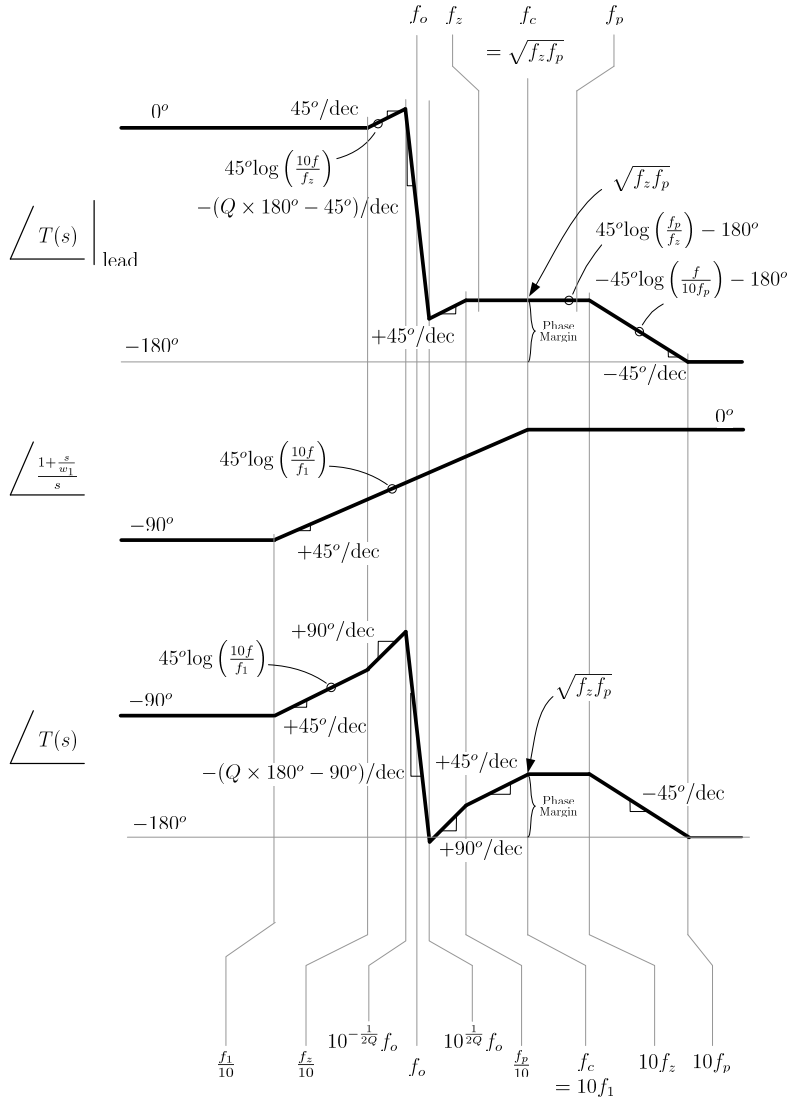


Figure 30: Bode Plot of Lead Compensator (500Hz)

Setting $R_1 = 100\text{K}$ and using the approximation $C_3 \ll C_2$ we find the component values:

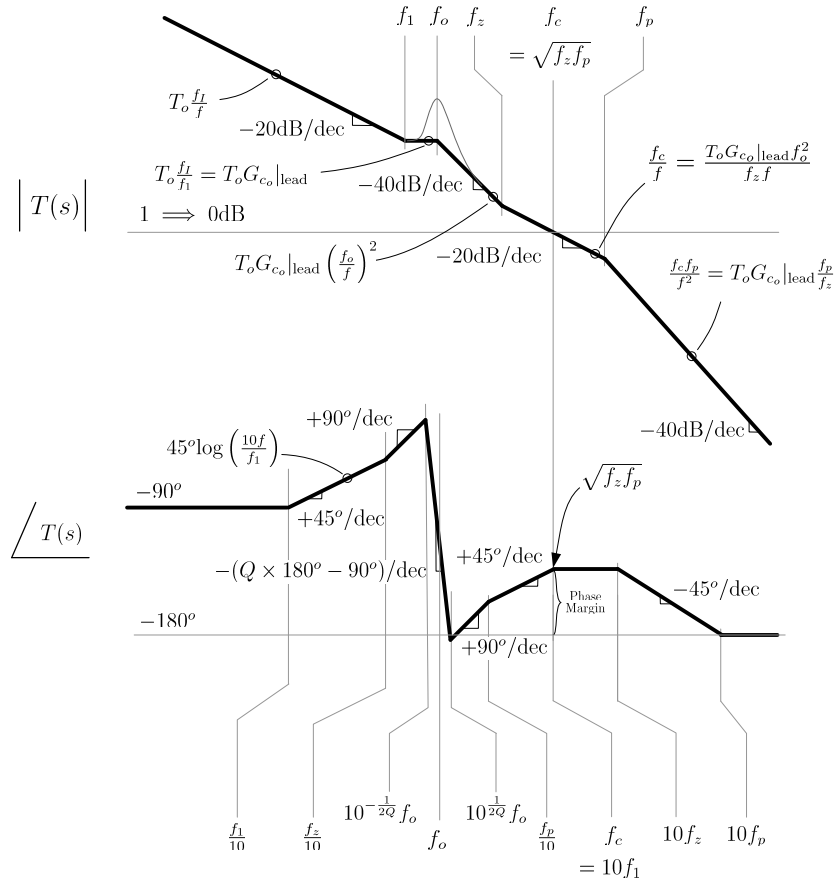


Figure 31: Bode Plot of System with Lead plus Integral Compensation (500Hz)

$$\begin{aligned}
 C_1 &= \frac{1}{\omega_z R_1} = 2.2nF \\
 C_2 &= \frac{1}{\omega_I R_1} = 1nF \\
 R_2 &= \frac{1}{\omega_1 C_2} = 330k\Omega \\
 C_3 &= \frac{1}{\omega_p R_2} = 33pF
 \end{aligned} \tag{32}$$

A PECS implementation of the closed loop system is shown in Fig. 34. The simulated response of input voltage steps $26V \rightarrow 30V \rightarrow 28V$ is shown in Fig. 35. Clearly seen here is the zero steady state error and a maximum voltage

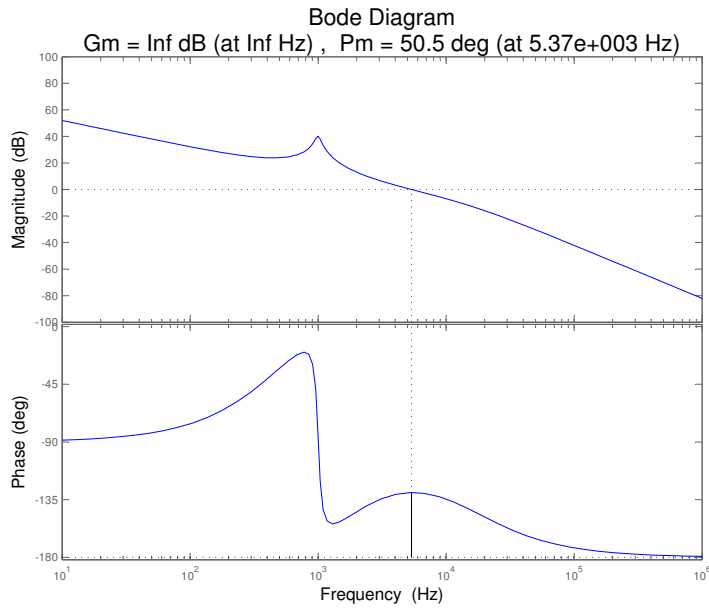


Figure 32: Matlab Lead Compensator with Integrator and Zero at 500Hz

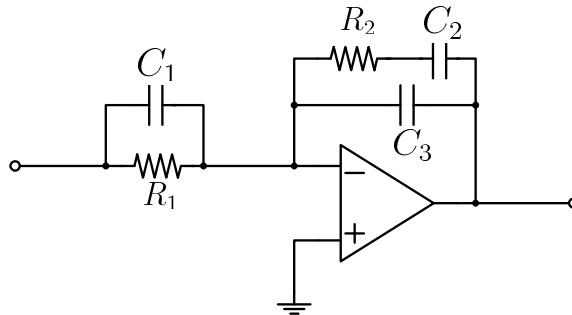


Figure 33: Compensator Circuit for Dominant Pole with Lead Compensation

deviation of around 80 mV with a settling time of around 1 ms.

7.2 Design 2: Zero $f_1 = 150$ Hz

The above design procedure will now be repeated for the case of the zero $f_1 = 150$ Hz. The resulting asymptotic phase plot construction is shown in Fig. 36. The final magnitude and phase asymptotic plots are given in Fig. 37. The new f_I is now found to be from (33)

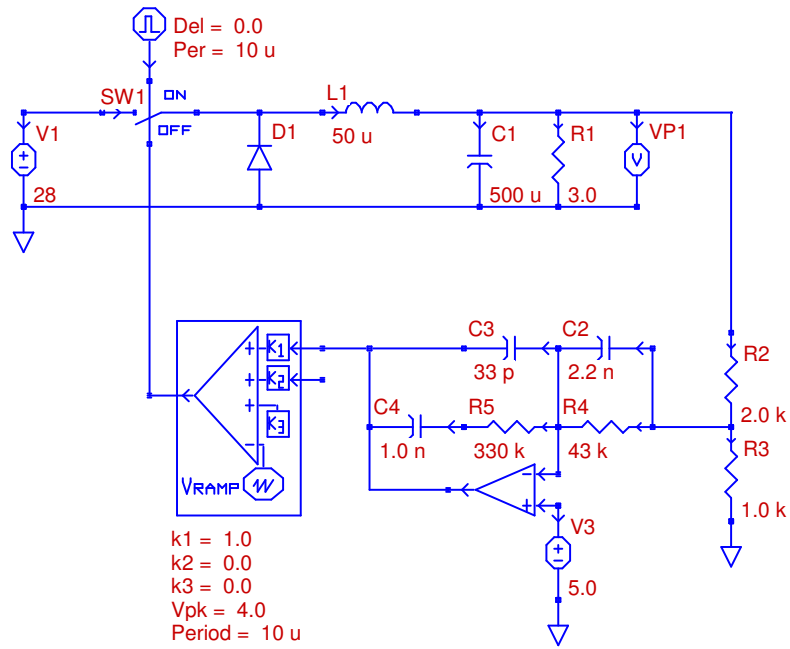


Figure 34: PECS Schematic of Lead Compensated System with Zero at 500Hz

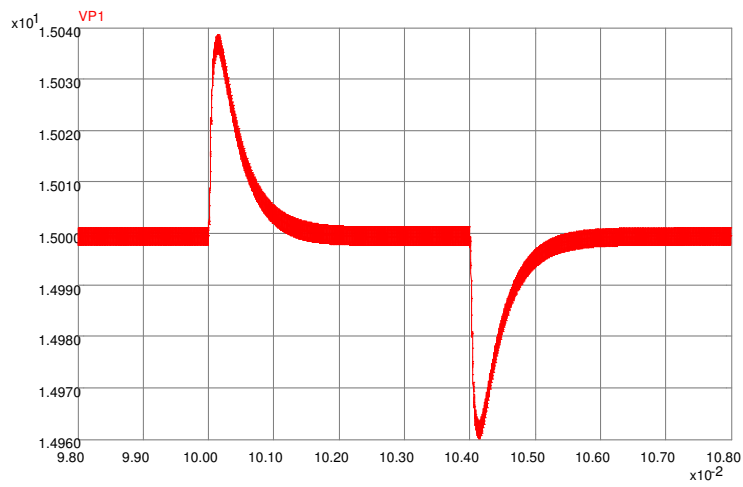


Figure 35: PECS Simulation of Lead Compensated System with Zero at 500Hz

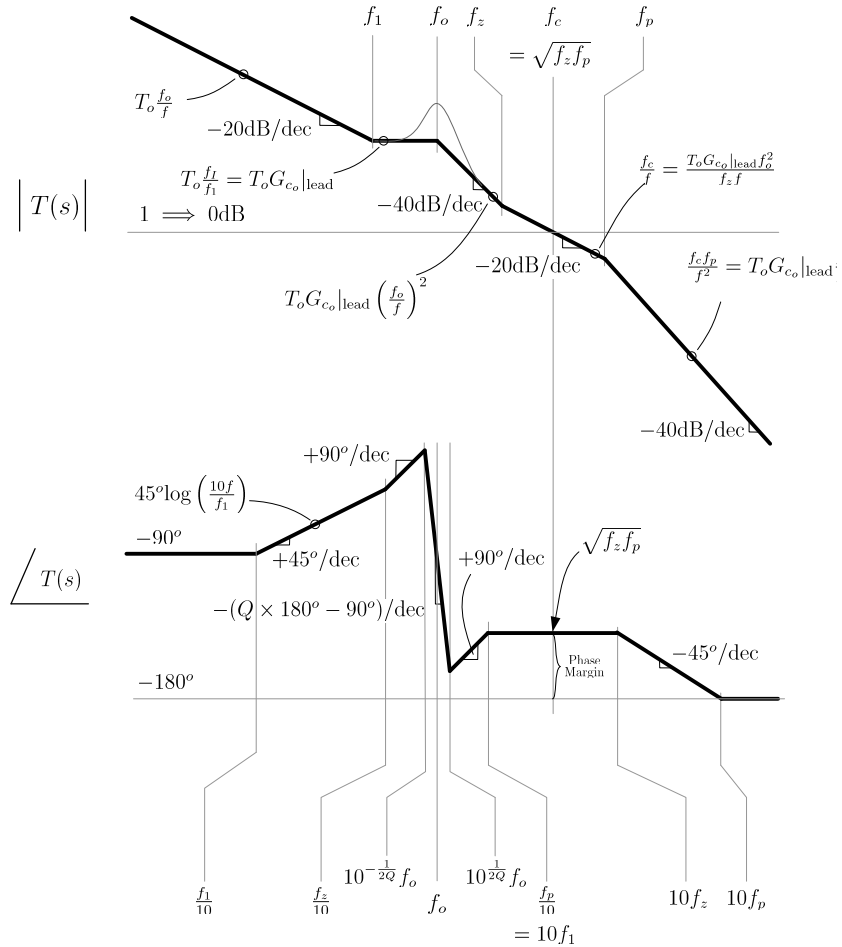


Figure 37: Bode Plot of System with Lead plus Integral Compensation (150Hz)

The change of $f_1 = 150\text{Hz}$ to $f_1 = 150\text{Hz}$ results in only a change in one capacitor value in the compensator. The resulting PECS implementation is shown in Fig. 39 along with the response of input voltage steps of $28\text{V} \rightarrow 30\text{V} \rightarrow 28\text{V}$, in Fig. 40. We now see that the peak voltage variation has slightly increased to 90mV but the settling time has tripled to around 3ms .

8 Extended Bandwidth Design

In the following we examine the performance of a compensator (closely related to the previous two) which is designed to produce an extended loop bandwidth. To this end a unity gain crossover frequency $f_c = 40\text{kHz}$ is, somewhat arbitrarily,

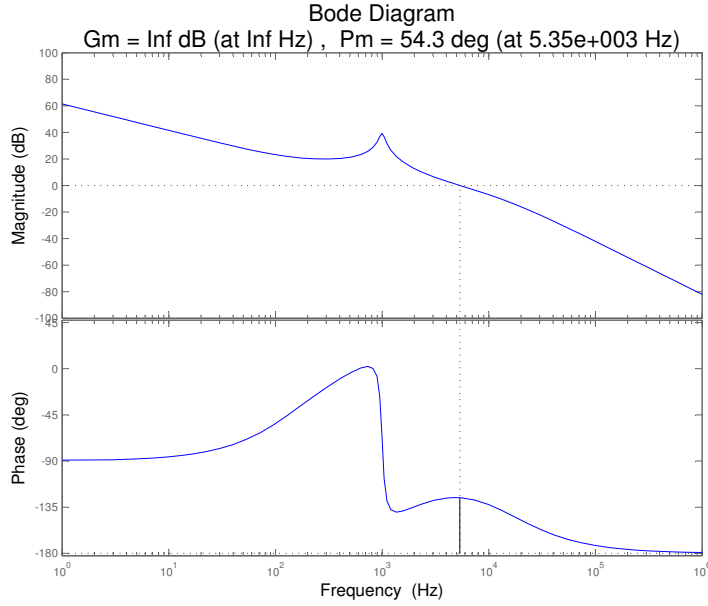


Figure 38: Matlab Lead Compensator with Integrator and Zero at 150Hz

chosen. The compensator used is

$$G_c(s) = \frac{\omega_I \left(1 + \frac{s}{\omega_{z1}}\right) \left(1 + \frac{s}{\omega_{z2}}\right)}{s} \quad (34)$$

The zeros $f_{z1} (= \frac{\omega_{z1}}{2\pi})$ and $f_{z2} (= \frac{\omega_{z2}}{2\pi})$ are simply chosen as follows. Zero f_{z2} is set so $f_{z2} = f_o$ so as to counter the effects of the plant complex pole pair. The lower frequency zero f_{z1} is set so that $f_{z1} = \frac{f_o}{10}$ to minimize the phase drop at f_o . The resulting loop gain expression is given by

$$T(s) = \omega_I T_o \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \left(1 + \frac{s}{\omega_{z2}}\right)}{s \left[1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2\right]} \quad (35)$$

The asymptotic magnitude and phase responses of the resulting loop gain are shown in Fig. 41, where the phase contributions of the different factors are individually drawn and then summed at the bottom plot to produce the overall asymptotic loop gain phase plot.

To determine the quantity $\omega_I (= 2\pi f_I)$ in (34) the high frequency asymptotes of the magnitude plot is used. At the crossover frequency f_c we have

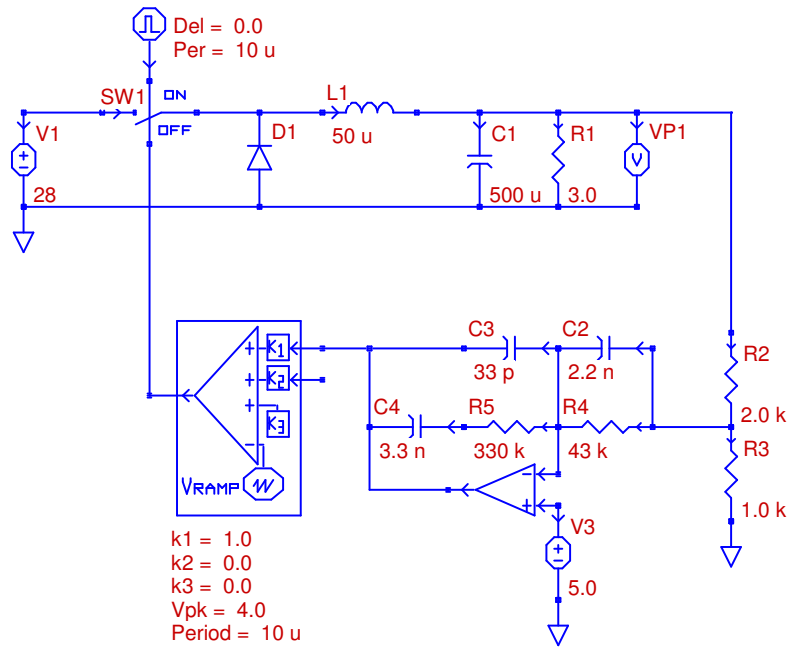


Figure 39: PECS Schematic of Lead Compensated System with Zero at 150Hz

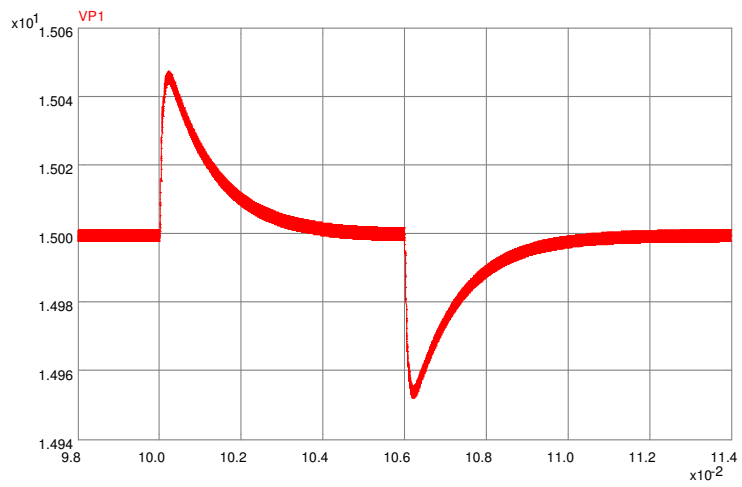


Figure 40: PECS Simulation of Lead Compensated System with Zero at 150Hz

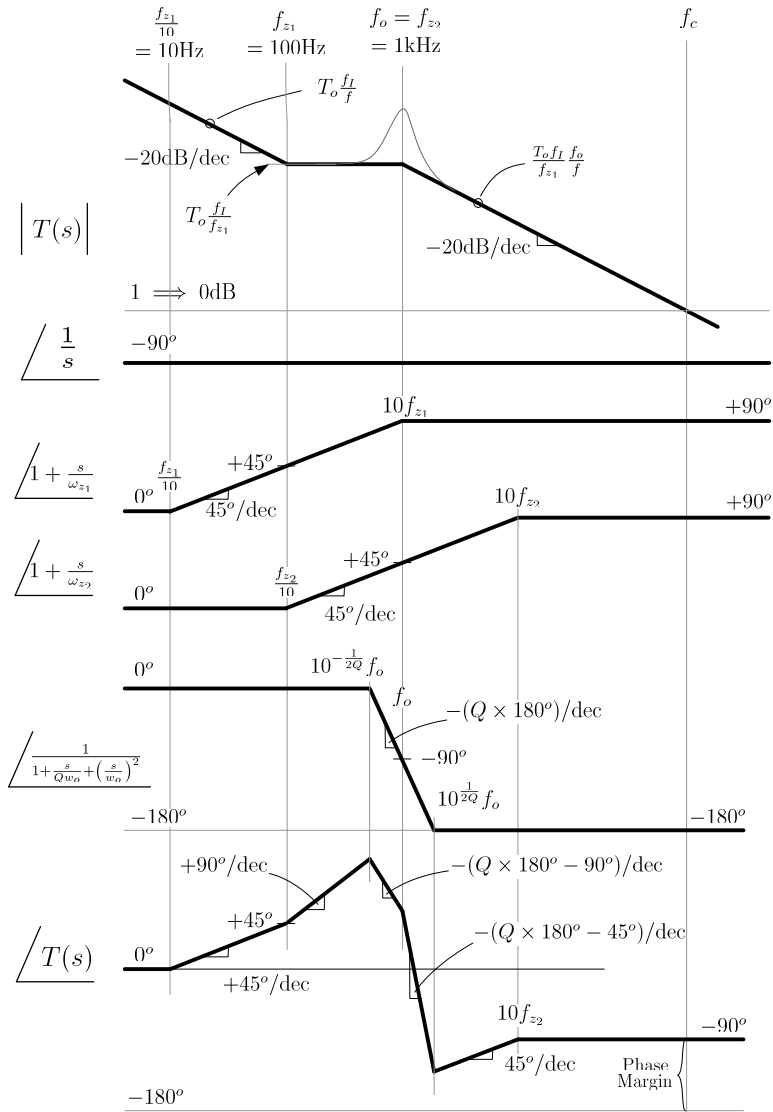


Figure 41: Extended Bandwidth Bode Plot and Phase Construction

$$\frac{T_o f_I f_o}{f_{z1} f_c} = 1 \quad (36)$$

so that we have

$$f_I = \frac{f_{z1} f_c}{T_o f_o} \quad (37)$$

with the values at hand we find

$$f_I = 172 \quad (38)$$

From the phase asymptotic plot of Fig. 41 we can clearly see that the expected phase margin is 90° . Using Matlab we more precisely find with the design values used $f_c = 40\text{kHz}$ and phase margin is 88.6° as shown in Fig. 42.

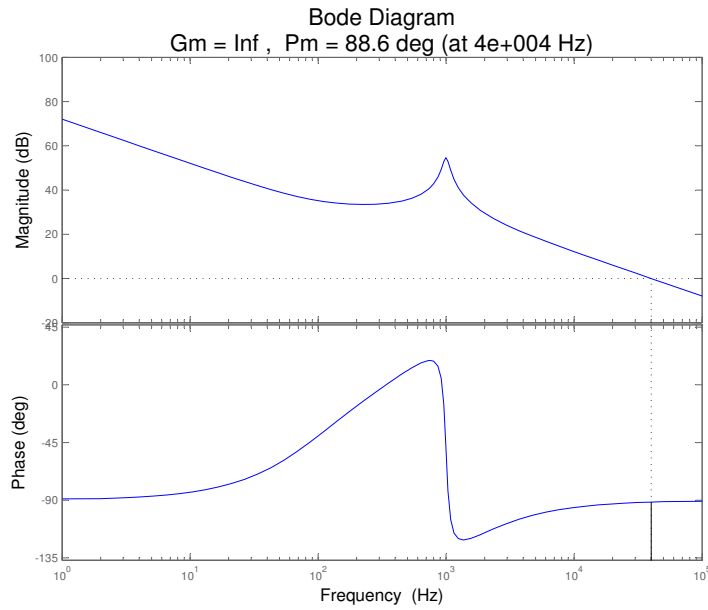


Figure 42: Matlab Analysis of Extended Compensator

The resulting PECS implementation is shown in Fig. 43 along with the response of input voltage steps of $28V \rightarrow 30V \rightarrow 28V$, in Fig. 44. We now see that the peak voltage variation has greatly reduced to just 30mV.

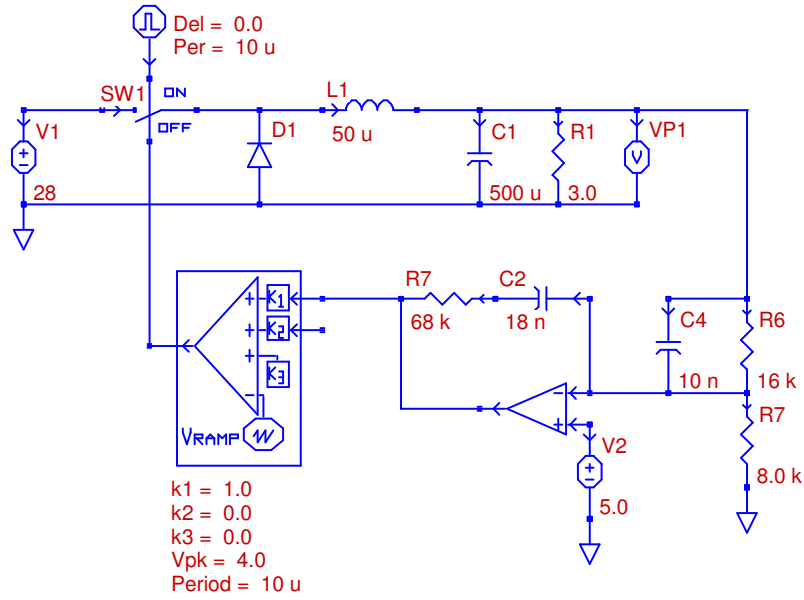


Figure 43: PECS Schematic of Extended System

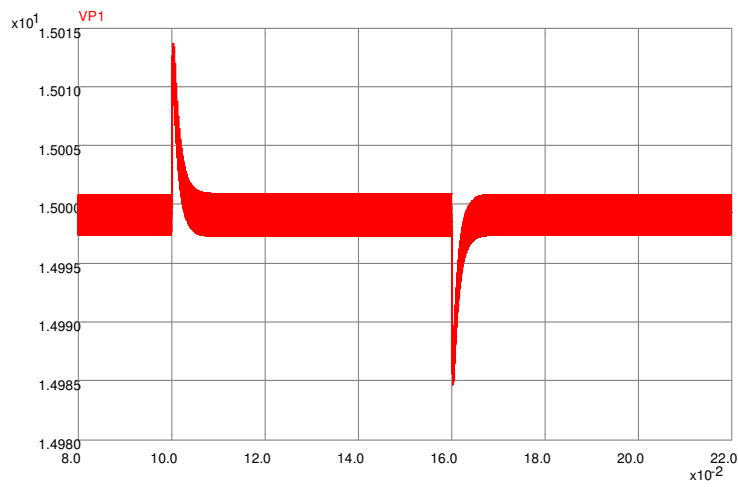


Figure 44: PECS Simulation of Extended System

9 Conclusion

The following table shows the summary of all of the results.

Table 2: Summary of Compensators
 Loop Gain $T(s) = G_c(s) \frac{T_o}{1 + Q\frac{s}{\omega_o} + (\frac{s}{\omega_o})^2}$,

where $T_o = 2.33$, $Q = 9.5$, and $\omega_o = 2\pi(1kHz)$

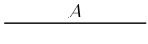
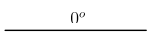
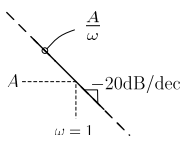
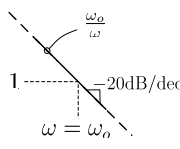
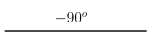
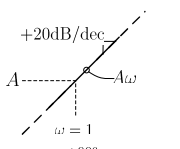
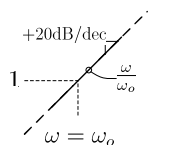
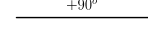
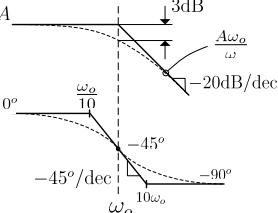
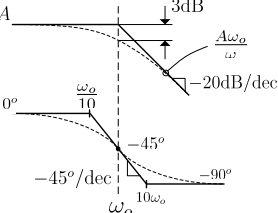
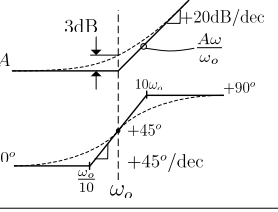
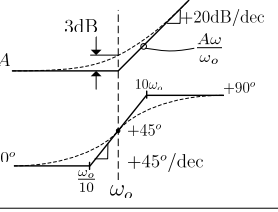
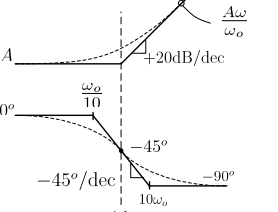
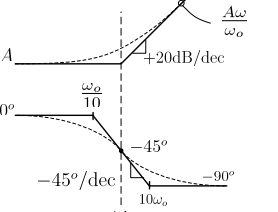
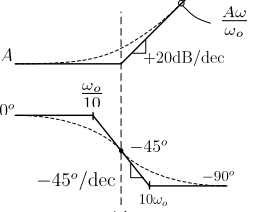
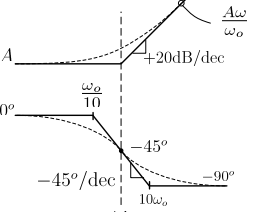
Compensator Design	Compensator Transfer Function $G_c(s)$	ϕ_M Asymptote (Matlab) (degrees)	f_c Asymptote (Matlab) (kHz)	Δv (mV)
Uncompensated Open Loop	G_{c_o} $G_{c_o} = 1$	0 (5)	1.5 (1.82)	2,800
Dominant Pole (3dB gain margin)	$\frac{\omega_I}{s}$ $\omega_I = 2\pi(32)$	90 (90)	0.0744 (0.0746)	3,700
Dominant Pole + Zero (10db gain margin)	$\frac{\omega_I(1 + \frac{s}{\omega_1})}{s}$ $\omega_I = 2\pi(14.3)$ $\omega_1 = 2\pi(1,000)$	90 (92)	0.0333 (0.033)	3,700
Lead	$G_{c_o} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}$ $G_{c_o} = 3.4$ $\omega_z = 2\pi(1,580)$ $\omega_p = 2\pi(15,800)$	45 (56)	5.0 (5.35)	120
Lead + Integrator + Zero at 500Hz	$\frac{\omega_I(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_z})}{s(1 + \frac{s}{\omega_p})}$ $\omega_I = 2\pi(1,770)$ $\omega_1 = 2\pi(500)$ $\omega_z = 2\pi(1,580)$ $\omega_p = 2\pi(15,800)$	45 (51)	5.0 (5.37)	80
Lead + Integrator + Zero at 150Hz	$\frac{\omega_I(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_z})}{s(1 + \frac{s}{\omega_p})}$ $\omega_I = 2\pi(351)$ $\omega_1 = 2\pi(150)$ $\omega_z = 2\pi(1,580)$ $\omega_p = 2\pi(15,800)$	45 (54)	5.0 (5.35)	90
Extended Bandwidth	$\frac{\omega_I(1 + \frac{s}{\omega_{z1}})(1 + \frac{s}{\omega_{z2}})}{s}$ $\omega_I = 2\pi(172)$ $\omega_{z1} = 2\pi(100)$ $\omega_{z2} = 2\pi(1000)$	90 (89)	40 (40)	30

References

- [1] Richard Tymerski, PECS Simulator ©1999-2009, Portland, Oregon, tymerski@ece.pdx.edu
- [2] Matlab, ©1984-2007, The MathWorks Inc., www.mathWorks.com
- [3] Robert W. Erickson and Dragan Maksimovic, Fundamentals of Power Electronics Second Edition. Springer Science+Business Media, LLC, 233 Spring Street, New York, NY 10013, USA, 2001.

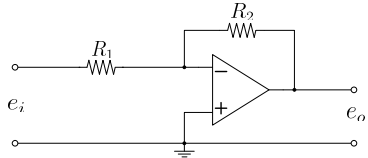
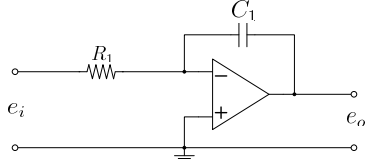
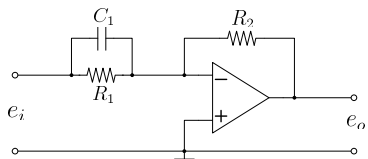
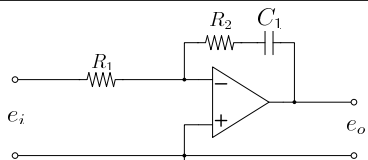
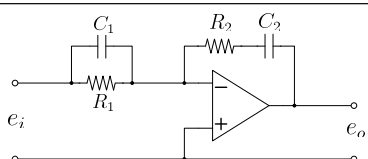
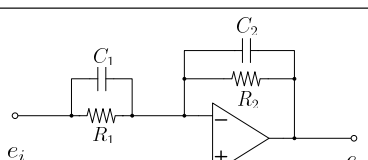
Appendix

9.1 Bode Plots

$H(s) = A$	$ H(s) $ 	
Simple Gain	$\angle H(s)$ 	
$H(s) = \frac{A}{s}$	$ H(s) $  Or: $H(s) = \frac{\omega_o}{s}$ $\omega_o = A$ 	
Pole at Zero	$\angle H(s)$ 	
$H(s) = As$	$ H(s) $  Or: $H(s) = \frac{s}{\omega_o}$ $\omega_o = \frac{1}{A}$ 	
Zero at Zero	$\angle H(s)$ 	
$H(s) = \frac{A}{1 + \frac{s}{\omega_o}}$	$ H(s) $  $\angle H(s)$ 	<p>(If $\omega \gg \omega_o$, $H(s) = \frac{A}{(\omega/\omega_o)} = \frac{A\omega_o}{\omega}$) Maximum Error @ $\omega_o = 3\text{dB}$ Maximum Error @ $\frac{\omega_o}{10}$ & $10\omega_o = 5.7^\circ$ Exact Phase: $-\tan^{-1}\left(\frac{\omega}{\omega_o}\right), \forall \omega$ Approx. Phase: $-45^\circ \log_{10}\left(\frac{10\omega}{\omega_o}\right), \frac{\omega_o}{10} \leq \omega \leq 10\omega_o$</p>
Pole at ω_o	$ H(s) $  $\angle H(s)$ 	<p>Maximum Error @ $\omega_o = 3\text{dB}$ Maximum Error @ $\frac{\omega_o}{10}$ & $10\omega_o = 5.7^\circ$ Exact Phase: $\tan^{-1}\left(\frac{\omega}{\omega_o}\right), \forall \omega$ Approx. Phase: $45^\circ \log_{10}\left(\frac{10\omega}{\omega_o}\right), \frac{\omega_o}{10} \leq \omega \leq 10\omega_o$</p>
Zero at ω_o	$ H(s) $  $\angle H(s)$ 	<p>Maximum Error @ $\omega_o = 3\text{dB}$ Maximum Error @ $\frac{\omega_o}{10}$ & $10\omega_o = 5.7^\circ$ Exact Phase: $-\tan^{-1}\left(\frac{\omega}{\omega_o}\right), \forall \omega$ Approx. Phase: $-45^\circ \log_{10}\left(\frac{10\omega}{\omega_o}\right), \frac{\omega_o}{10} \leq \omega \leq 10\omega_o$</p>
Right Half Plane Zero at ω_o	$ H(s) $  $\angle H(s)$ 	<p>Maximum Error @ $\omega_o = 3\text{dB}$ Maximum Error @ $\frac{\omega_o}{10}$ & $10\omega_o = 5.7^\circ$ Exact Phase: $-\tan^{-1}\left(\frac{\omega}{\omega_o}\right), \forall \omega$ Approx. Phase: $-45^\circ \log_{10}\left(\frac{10\omega}{\omega_o}\right), \frac{\omega_o}{10} \leq \omega \leq 10\omega_o$</p>

$H(s) = \frac{A}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2}$ <p>Second Order Complex Pole</p>		$\omega_o = \text{Corner Frequency}$ $Q > \frac{1}{2} \implies \text{Complex Roots}$ $Q = \text{Quality Factor: Exact Gain @ } \omega_o$ Approximate Maximum Value $\text{Exact Phase: } -\tan^{-1} \left[\frac{\frac{1}{Q} \frac{\omega}{\omega_o}}{1 - \left(\frac{\omega}{\omega_o}\right)^2} \right], \forall \omega$
$H(s) = A \left(1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2 \right)$ <p>Second Order Complex Zero</p>		$\omega_o = \text{Corner Frequency}$ $Q > \frac{1}{2} \implies \text{Complex Roots}$ $\text{Exact Phase: } \tan^{-1} \left[\frac{\frac{1}{Q} \frac{\omega}{\omega_o}}{1 - \left(\frac{\omega}{\omega_o}\right)^2} \right], \forall \omega$

9.2 Compensator Circuits

	Control Action	$G(s) = \frac{E_o(s)}{E_i(s)}$	Operational Amplifier Circuits
1	P Proportional	$-A$ where: $A = \frac{R_2}{R_1}$	
2	I Integral	$-\frac{1}{s/\omega_0}$ where: $\omega_0 = \frac{1}{R_1 C_1}$	
3	PD Proportional-Derivative	$-A(1 + \frac{s}{\omega_1})$ where: $A = \frac{R_2}{R_1}, \quad \omega_1 = \frac{1}{R_1 C_1}$	
4	PI Proportional-Integral	$-A \frac{1 + \frac{s}{\omega_1}}{\frac{s}{\omega_1}}$ where: $A = \frac{R_2}{R_1}, \quad \omega_1 = \frac{1}{R_2 C_1}$	
5	PID Proportional-Integral-Derivative	$-A \frac{(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2})}{\frac{s}{\omega_2}}$ where: $A = \frac{R_2}{R_1}, \quad \omega_1 = \frac{1}{R_1 C_1}, \quad \omega_2 = \frac{1}{R_2 C_2}$	
6	Lead if $\omega_1 < \omega_2$ or Lag if $\omega_1 > \omega_2$	$-A \frac{1 + \frac{s}{\omega_1}}{1 + \frac{s}{\omega_2}}$ where: $A = \frac{R_2}{R_1}, \quad \omega_1 = \frac{1}{R_1 C_1}, \quad \omega_2 = \frac{1}{R_2 C_2}$	

	Control Action	$G(s) = \frac{E_o(s)}{E_i(s)}$	Operational Amplifier Circuits
7	Lead-Lag	$-A \frac{(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2})}{(1 + \frac{s}{\omega_3})(1 + \frac{s}{\omega_4})}$ <p>where:</p> $A = \frac{R_4}{R_3},$ $\omega_1 = \frac{1}{(R_1 + R_3)C_1}, \quad \omega_2 = \frac{1}{R_2 C_2}$ $\omega_3 = \frac{1}{R_1 C_1}, \quad \omega_4 = \frac{1}{(R_2 + R_4)C_2}$	
8	Integrator with Lead or Lag	<p>where:</p> $\omega_0 = \frac{1}{R_1(C_1 + C_2)}$ $\omega_1 = \frac{1}{R_2 C_2}$ $\omega_2 = \frac{1}{R_2 \frac{C_1 C_2}{C_1 + C_2}}$	
9	Integrator with Lead	<p>where:</p> $\omega_0 = \frac{1}{R_1(C_2 + C_3)}$ $\omega_1 = \frac{1}{R_2 C_2}, \quad \omega_2 = \frac{1}{R_1 C_1}$ $\omega_3 = \frac{1}{R_2 \frac{C_2 C_3}{C_2 + C_3}}$	
10	Integrator with Lead-Lag	<p>where:</p> $\omega_0 = \frac{1}{R_1(C_2 + C_3)}$ $\omega_1 = \frac{1}{R_2 C_2}, \quad \omega_2 = \frac{1}{C_1(R_1 + R_3)},$ $\omega_3 = \frac{1}{R_3 C_1}, \quad \omega_4 = \frac{1}{R_2 \frac{C_2 C_3}{C_2 + C_3}}$	